

WHAT IS CLAIMED IS:

el 23  
1. A thin-film transistor comprising a semiconductor layer and multiple gate electrodes that have been formed over the semiconductor layer,

wherein the semiconductor layer includes:

23a 28b  
first and second heavily doped regions, which have a first conductivity type, are spaced apart from each other and serve as source/drain regions;

20a 20b  
a plurality of channel regions, which have a second conductivity type, are located between the first and second heavily doped regions so as to face the gate electrodes, and include first and second channel regions, wherein the first channel region is closer to the first heavily doped region than any other one of the channel regions is, while the second channel region is closer to the second heavily doped region than any other one of the channel regions is;

22  
an intermediate region, which has the first conductivity type and is located between two mutually adjacent ones of the channel regions;

26a  
a first lightly doped region, which has the first conductivity type and is located between the first channel region and the first heavily doped region;

26b  
a second lightly doped region, which has the first conductivity type and is located between the second channel region and the second heavily doped region;

a third <sup>24a</sup> lightly doped region, which has the first conductivity type, has a carrier concentration different from that of the first <sup>26a</sup> lightly doped region and is located between the first <sup>262</sup> lightly doped region and the first <sup>20a</sup> channel region; and

a fourth <sup>24b</sup> lightly doped region, which has the first conductivity type, has a carrier concentration different from that of the second <sup>26b</sup> lightly doped region and is located between the second <sup>26b</sup> lightly doped region and the second <sup>20b</sup> channel region.

2. The transistor of claim 1, wherein the first and second heavily doped regions have substantially the same carrier concentration;

the first and second lightly doped regions also have substantially the same carrier concentration;

the third and fourth lightly doped regions and the intermediate region also have substantially the same carrier concentration;

the carrier concentration of the first heavily doped region is substantially higher than that of the first lightly doped region; and

the carrier concentration of the first lightly doped region is substantially higher than that of the third lightly doped region.

3. The transistor of claim 1, wherein the channel regions, the intermediate region and the third and fourth lightly doped regions of the semiconductor layer have been doped with a dopant of the second conductivity type at substantially the same dose.

4. The transistor of claim 3, wherein the third and fourth lightly doped regions have been doped not only with the dopant of the second conductivity type but also the same dopant of the first conductivity type as a dopant that has been introduced into the first and second lightly doped regions.

5. The transistor of claim 4, wherein a difference between the carrier concentration of the third lightly doped region and that of the first lightly doped region is caused by the dopant of the second conductivity type that has been introduced into the third lightly doped region.

6. The transistor of claim 4, wherein a difference between the carrier concentration of the fourth lightly doped region and that of the second lightly doped region is caused by the dopant of the second conductivity type that has been introduced into the fourth lightly doped region.

7. The transistor of claim 1, wherein the first and second lightly doped regions have substantially the same length.

8. The transistor of claim 1, wherein the third and fourth lightly doped regions have substantially the same length.

9. The transistor of claim 1, wherein the intermediate region has a length smaller than a total length of the first and third lightly doped regions.

10. The transistor of claim 1, wherein the intermediate region has a length smaller than a total length of the second and fourth lightly doped regions.

11. A method for fabricating a thin-film transistor, comprising the steps of:

forming a semiconductor thin film on an insulating substrate;

doping a first region of the semiconductor thin film, which includes a part that will serve as a channel region, with a first dopant of a first conductivity type;

forming at least one gate electrode on the semiconductor thin film so that the part of the semiconductor thin film

that will serve as the channel region is covered with the gate electrode;

selectively doping a second region of the semiconductor thin film with a second dopant of a second conductivity type using the gate electrode as a mask, the second region including other parts of the first region, except the part that will serve as the channel region, and other parts of the semiconductor thin film that surround the first region; and

doping a third region of the semiconductor thin film with a third dopant of the second conductivity type, thereby defining regions that will serve as source/drain regions, the third region being so defined as to be spaced apart, by a predetermined distance, from an outer edge of parts of the semiconductor thin film where the first and second region overlap with each other.

12. The method of claim 11, wherein the second and third regions overlap with each other at least partially.

13. The method of claim 11, wherein an implant dose of the second dopant is smaller than an implant dose of the third dopant.

14. A thin-film transistor comprising a semiconductor layer and multiple gate electrodes that have been formed over

the semiconductor layer,

wherein the semiconductor layer includes:

first and second heavily doped regions, which are spaced apart from each other and serve as source/drain regions;

a plurality of channel regions, which are located between the first and second heavily doped regions so as to face the gate electrodes and which include first and second channel regions, wherein the first channel region is closer to the first heavily doped region than any other one of the channel regions is, while the second channel region is closer to the second heavily doped region than any other one of the channel regions is;

an intermediate region located between two mutually adjacent ones of the channel regions;

a first lightly doped region located between the first channel region and the first heavily doped region; and

a second lightly doped region located between the second channel region and the second heavily doped region, and

wherein the first channel region includes a first intrinsic channel region and the second channel region includes a second intrinsic channel region.

15. The transistor of claim 14, wherein the first and second intrinsic channel regions are substantially covered with associated ones of the gate electrodes.

16. The transistor of claim 14, wherein the first channel region includes a doped channel region between the first intrinsic channel region and the intermediate region, while the second channel region includes a doped channel region between the second intrinsic channel region and the intermediate region.

17. The transistor of claim 16, wherein the respective doped channel regions of the first and second channel regions and the intermediate region have been doped with a dopant of a first conductivity type at a predetermined dose.

18. The transistor of claim 14, wherein the first and second lightly doped regions have substantially the same length.

19. The transistor of claim 14, wherein the first and second intrinsic channel regions have substantially the same length.

20. The transistor of claim 14, wherein the first and second intrinsic channel regions are each shorter than any of the intermediate region, the first lightly doped region and the second lightly doped region.

10020440-121801

21. A method for fabricating a thin-film transistor, comprising the steps of:

forming a semiconductor thin film on an insulating substrate;

doping a first region of the semiconductor thin film with a first dopant of a first conductivity type;

forming at least one gate electrode on the semiconductor thin film so that a part of the first region and a part of the semiconductor thin film that surrounds the first region are covered with the gate electrode;

selectively doping a second region of the semiconductor thin film with a second dopant of a second conductivity type using the gate electrode as a mask, the second region including at least a part of the first region and other parts of the semiconductor thin film that surround the first region and that are not covered with the gate electrode; and

doping a fourth region of the semiconductor thin film with a third dopant of the second conductivity type, the fourth region being so defined as to be spaced apart from a third region of the semiconductor thin film by a predetermined distance, the third region including at least the part of the first region and the part of the semiconductor thin film that is covered with the gate electrode.

22. The method of claim 21, wherein the second and fourth regions overlap with each other at least partially.

Sub  
A1  
23. An active-matrix-addressed liquid crystal display device comprising:

10020440 121801  
a substrate, on which the thin-film transistor according to claim 1 or 14; a data bus line electrically connected to the first heavily doped region of the thin-film transistor; a gate bus line electrically connected to at least one of the gate electrodes of the thin-film transistor; and a pixel electrode electrically connected to the second heavily doped region of the thin-film transistor have been formed, and

add  
A2  
a liquid crystal layer, which has an optical state changeable with a potential level at the pixel electrode.